MEMORY SYSTEM

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CI-1103-2

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TECHNICAL MANUAL

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MEMORY SYSTEM

CI-1108-2

PRELIMINARY
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SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation, instalation, and design of the CI-1103-2 dynamic read/write memory.

1.2 THE MEMORY MODULE

The CI-1103-2 various options are summarized below:

OPTION	MEMORY CAPACITY	MEMORY CHIP UTILIZED
16K	16K by 16 or 18 bits	16K by 1 (4116)
32K	32K by 16 or 18 bits	16K by 1 (4116)

1.2.1 CI-1103-2 MEMORY DESCRIPTION

The CI-1103 is a high speed, high density dynamic read/write memory which is plug compatible with the DEC LSI 11/2, LSI 11/23, PDP-1103, and PDP-1123. Memory storage is provided by 16K by 1 dynamic MOS memory chips. The memory is a single package plug-in module having dimensions of 8.44" x 5.187".

1.2.2 OPTIONAL FEATURES

The memory module contains its own address and data buffers. Address, data-in and data-out are multiplexed for bus compatibility with the Q-Bus. The system memory address space to which the module will respond is user-confisured via switches contained on the module. An address can be selected in 4K increments through the 0-4 Megabyte address range. The module contains its own complete refresh control logic requiring no outside intervention. The module generates and checks even parity which is totally DEC hardware and software compatible.

1.2.4 POWER REQUIREMENTS

The memory module requires a 5 volt and 12 volt power source supplied by the system.

1.3 GENERAL SPECIFICATION REQUIREMENTS

Table 1.3.1 lists the general specifications for the CI-1103-2 memory.

TABLE 1.3.1

CHARACTERISTICS	SPECIFICATIONS
Capacity	16KW to 32KW x 16 or 18 bits
Cycle Time	400 nanoseconds
Access Time	240 nanoseconds from sync active
Word Size	16 bits
Address	22 bits (random access)
Data-in/Data-out	16 bits bidirectional with open collector TTL voltage compatible
Modes of Operation	DATO, DATOB, DATI, DATIO, DATIOB
Expansion	4KW Memory Blocks up to 4 Megabyte by selecting the proper switch
Refresh	On Board distributed
Parity	Even
Interface Signals	
Inputs	TTL Compatible
Outputs	Open Collector
Operating Temperature	0 to 60 DEG C
Storage Temperature	-20 to 70 DEG C
Power Requirements	MODE: NORMAL (Operate / Standby), BACKUP (Operate / Standby)
+5.0V	1.2A / 900mA / 600mA / ---
+5VB	--- / --- / 600mA / 300mA
+12V	300mA / 80mA / --- / ---
+12VB	300mA / 80mA / 300mA / 80mA
Dimensions	8.44" x 5.187"

1.4 MEMORY ADDRESS SELECTION

(Refer to drawing 70554 for switch and PEG location)

1.4.1 Option 1 - 4K WORD INCREMENT SELECTION

The CI-1103-2 is shipped in OPTION 1 configuration. In this configuration the placement of PEG in AREA A enables selection of the lower 64KW of memory (000000 to 377777, PEG between posts 1 and 2) or the selection of the upper 64KW of memory (400000 to 777777, PEG between posts 2 and 3). The selection of the memory is performed in 4K increments in either the lower or the upper 64KW of memory by closing the appropiate switches per table 1.4.1.

TABLE 1.4.1

BANK SELECTED AREA A PEG POSITION 1 - 2	BANK SELECTED AREA A PEG POSITION 2 - 3	CLOSED SWITCH	BANK SELECTED AREA A PEG POSITION 1 - 2	BANK SELECTED AREA A PEG POSITION 2 - 3	CLOSED SWITCH
000000 to 017777	400000 to 417777	SW1-1	200000 to 217777	600000 to 617777	SW2-1
020000 to 037777	420000 to 437777	SW1-2	220000 to 237777	620000 to 637777	SW2-2
040000 to 057777	440000 to 457777	SW1-3	240000 to 257777	640000 to 657777	SW2-3
060000 to 077777	460000 to 477777	SW1-4	260000 to 277777	660000 to 677777	SW2-4
100000 to 117777	500000 to 517777	SW1-5	300000 to 317777	700000 to 717777	SW2-5
120000 to 137777	520000 to 537777	SW1-6	320000 to 337777	720000 to 737777	SW2-6
140000 to 157777	540000 to 557777	SW1-7	340000 to 357777	740000 to 757777	SW2-7
160000 to 177777	560000 to 577777	SW1-8	360000 to 377777	760000 to 777777	SW2-8

NOTE: 1. On the 16K option a total of 4 switches can be closed and should be contiguous.
2. On the 32K option a total of 8 switches can be closed and should be contiguous.

OPTION 2 - 8K WORD INCREMENT SELECTION

The CI-1103-2 can be reconfigured for OPTION 2 selection per APPENDIX A. In this configuration PEG in AREA A is placed between posts 2 and 4. The memory is selected in 8KW increments by closing the appropriate switches per table 1.4.2.

TABLE 1.4.2

BANK SELECTED	CLOSED SWITCH	BANK SELECTED	CLOSED SWITCH
000000 to 037777	SW1-1	400000 to 437777	SW2-1
040000 to 077777	SW1-2	440000 to 477777	SW2-2
100000 to 137777	SW1-3	500000 to 537777	SW2-3
140000 to 177777	SW1-4	540000 to 577777	SW2-4
200000 to 237777	SW1-5	600000 to 637777	SW2-5
240000 to 277777	SW1-6	640000 to 677777	SW2-6
300000 to 337777	SW1-7	700000 to 737777	SW2-7
340000 to 377777	SW1-8	740000 to 777777	SW2-8

NOTES:
1. On the CI-1103-2 32K option a total of 4 switches can be closed, and the memory field selected should be contiguous.
2. On the CI-1103-2 16K option a total of 2 switches can be closed, and the memory field selected should be contiguous.
3. See APENDIX A for reconfiguration from memory select OPTION 1 to memory select OPTION 2.

1.4.3 BANK 7 2KW SELECTION OPTION

The CI-1103-2 is disabled whenever the BBS7L SIGNAL is asserted on the bus. The lower 2K portion of BANK 7 can enabled by moving PEG in AREA B from posts 2 and 3 to posts 1 and 2.

NOTE: User must take caution to insure no I/O devices utilize the lower 2KW portion of BANK 7 or bus contention will occur resulting in improper system operation.

1.4.4 EXTENDED MEMORY SELECTION TO 4 MEGABYTES

For extended memory selection implementation see APPENDIX A.

SECTION 2

HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section details handling precautions. It includes step by step procedures to interface the CI-1103-2 memory with the LSI-11/23 and the PDP-1123 microcomputer family.

2.2 HANDLING PRECAUTIONS

The memory IC's used on the CI-1103-2 are MOS devices. They can be damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC. Also avoid unnecessary handling and wear cotton--rather than synthetic--clothing when you do handle these IC's.

2.3 INTERFACE SIGNALS

The input signals to the memory are TTL compatible and the output signals are open collector. The timing relationship betwen these signals are shown in figure 2.1.

2.4 INTERFACE WITH THE LSI 11/2, PDP-1103, 11/23 OR PDP-1123

The CI-1103-2 memory module may be installed in any slot available in the PDP-1103 or PDP-1123.

CAUTION: The memory module and backplane connector can be damaged if the module is installed backwards. Care should be taken to insure that the module is installed so that the component side of the module faces the same direction as other LSI-11 modules.

DC power must be removed from the backplane during module removal or insertion.